DESIGN AND PROCESS SENSITIVITY OF A TWO STAGE 6-18 GHz MONOLITHIC FEEDBACK AMPLIFIER

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ABSTRACT

The design of a 6-18 GHz, two stage monolithic feedback amplifier is discussed, and the critical process and FET parameters are identified. Variations in circuit performance experienced during a pilot production run are correlated with the predictions of a sensitivity analysis. The critical parameters are substrate height, GaAs sheet resistivity, gate-source capacitance, transconductance, and drain-source resistance. Measured results show the importance of substrate height and sheet resistivity in the control of gain flatness.

INTRODUCTION

Understanding the effects of material and process parameter variations on circuit performance is crucial to the development of high volume MMIC manufacturing capability. At Texas Instruments we have evaluated the rf performance of two-stage monolithic feedback amplifier chips from over 60 slices. In this paper we focus on efforts to control the gain ripple of pilot production chips made using our most recent design.

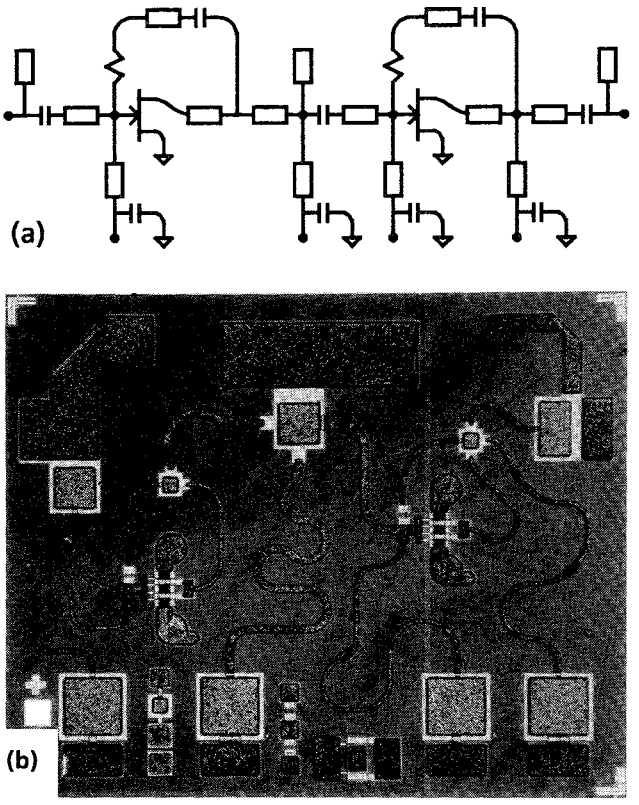

Figure 1. The EG8005 two-stage feedback amplifier, (a) schematic, (b) photograph.

DESIGN DESCRIPTION

The monolithic feedback amplifier shown in Fig. 1 is designed for use as a broadband, low to medium power gain stage in electronic warfare applications. Henceforth we refer to the device by its Texas Instruments Equipment Group part number, EG8005. Feedback is used as a mechanism for gain flattening and VSWR reduction, and the cascaded, common source configuration enables the device to attain more than 10 dB gain across the 6-18 GHz band with medium power-added efficiency. Some EG8005 devices have achieved 17% p.a.e. at 18 GHz, when operated with 21 dBm output power at 1 dB gain compression. All blocking and bypass capacitors are provided on-chip. This design is a second iteration of the design presented in Ref. 1; the performance deficiencies of the original design have been corrected along with a substantial reduction in chip area. Basic design data are shown in Table 1.

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Table 1: EG8005 Design Data

Chip Size: 92 x 75 mil

# of chips / slice	slice diameter	effective diameter
271	2 inch	1.8 inch
701	3 inch	2.8 inch
	(allows for 6 mil saw streets and 10 test bars per slice)	

Substrate thickness:	4.0 mil
Passivation/ Capacitor Dielectric:	2000 Å Silicon Nitride
Via Hole Diameter:	2.0 mil

The signal path in Fig. 1(b) is from left to right. The FET gatewidths are 300 µm. The two GaAs mesa feedback resistors can be seen near the gate pads. Only microstrip structures are used as tuning elements; there are no MIM or interdigitated tuning capacitors in the circuit. Gate and drain bias is applied through the four bond pads along the bottom of the chip. The square structures above the bond pads are 15 pF MIM bypass capacitors. The chip contains 85 pF of on-chip blocking and bypass capacitance.

PERFORMANCE-PROCESS INTERACTIONS

Gain responses of sample chips from an early slice, designated as slice A, are shown in Fig. 2. All samples were measured at a standard bias condition: – 1.0 V gate to source and + 6.0 V drain to source. The chips were selected on the basis of similar DC FET characteristics; the I_{dss} values for all the 300 µm FETs in each sample fell between 75 mA and 95 mA. The worst case gain ripple for the sample is 5.08 dB and the average is 4.25 dB, over 6-19 GHz. A severe dip in the gain is apparent at 9.5 GHz.

Computer modeling of the circuit design resulted in the identification of five parameters that need to be well controlled in order to maintain consistent circuit performance: FET intrinsic transconductance, g_m, gate-source capacitance, C_{gs}, drain-source resistance, R_{ds}, GaAs sheet resistivity, r_s, and substrate height, h_s. A sensitivity matrix for the gain response at various frequencies is listed in Table 2. The values in the table are estimates of the sensitivity factor S_G^{α} given by

$$S_G^{\alpha} = \frac{\alpha}{|S_{21}|} \frac{\partial |S_{21}|}{\partial \alpha}$$

where α is the parameter of interest and $|S_{21}|$ is the voltage gain of the amplifier. The sensitivity factors were obtained by perturbing the parameters in the computer model ± 10% and using a discrete approximation for the partial derivative. The factors can be thought of in this way: a 10% change in the parameter α causes a $10 \times S_G^{\alpha}$ percent change in voltage gain. Another example of sensitivity analysis is given in Ref. 2. The normalized sensitivity factors provide a basis for the comparison of the sensitivities of different designs.

Table 2: Voltage Gain Sensitivity Factors

$$S_G^{\alpha} = \frac{\alpha}{|S_{21}|} \frac{\partial |S_{21}|}{\partial \alpha}$$

parameter (α)	6.0 GHz	9.5 GHz	13.5 GHz	16.5 GHz	18.0 GHz
g_m	1.52	1.72	1.67	1.79	1.82
C_{gs}	0.02	-0.30	-0.77	-1.06	-1.05
R_{ds}	0.38	0.26	0.48	0.41	0.43
r_s	0.99	0.48	0.39	0.05	0.00
h_s	0.01	0.58	0.34	0.12	-0.06

The effects of each type of parameter variation can be seen clearly in the matrix. Increases in transconductance simply translate the gain upward, although the effect is not completely uniform. Increases in gate-source capacitance reduce the high end gain, but affect the low end very little. Increases in drain-source resistance tend to accentuate the gain peak at 13.5 GHz and the dip at 9.5 GHz. Changes in the sheet resistivity of the active GaAs layer affect the values of the feedback resistors (such changes affect the FET characteristics as well, but here the FET parameters are treated separately). Feedback is significant only in the lower half of the 6-18 GHz band; the effect of feedback resistor changes on the high end gain is negligible. Increases in sheet resistivity reduce the feedback effect, accentuating

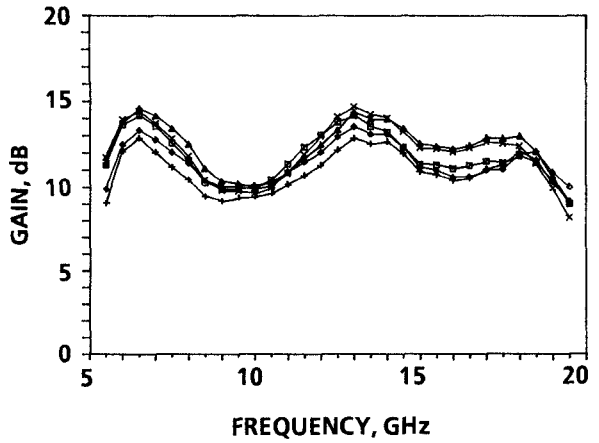

Figure 2. Measured gain responses of selected amplifiers from slice A. All devices measured at V_{GS} = -1.0 V, V_{DS} = +6.0 V.

both the low end peak and the dip at 9.5 GHz. Another prime suspect for the cause of the dip in gain at 9.5 GHz is the substrate height, which affects the dip region strongly.

Table 3 lists the values of the critical parameters assumed in the design, the values obtained from measurements of slice A, and values obtained from a subsequent slice, designated as slice B. The computer model responses for these three cases are shown in Fig. 3, and the measured responses of the slice B amplifier samples are shown in Fig. 4. Transconductance and the drain source resistance, R_{ds}, were calculated from low frequency (100-400 MHz) scalar scattering parameter measurements of two sample FETs from each slice, neglecting the capacitive reactances and using DC values for the source and drain parasitic resistances, R_s and R_d. The sample FETs were selected to have DC characteristics similar to those in the amplifier sample. The value of gate source capacitance for the two slices was simply adjusted to reflect the measured gain-slope characteristics of the amplifier samples. The sheet resistivity variations were determined from measurements of the GaAs feedback resistors. A sample of five non-functional chips from the two slices was selected at random and cleaved in half for optical substrate height measurements. All the samples fell within ±0.2 mils of the average value.

As can be seen in Fig. 3, despite careful attention to detail in the computer model of the circuit layout, we have been unable to predict all of the measured gain ripple. However, the trends predicted by the sensitivity analysis can be seen in the responses from slice B. The reduction in the feedback resistor values

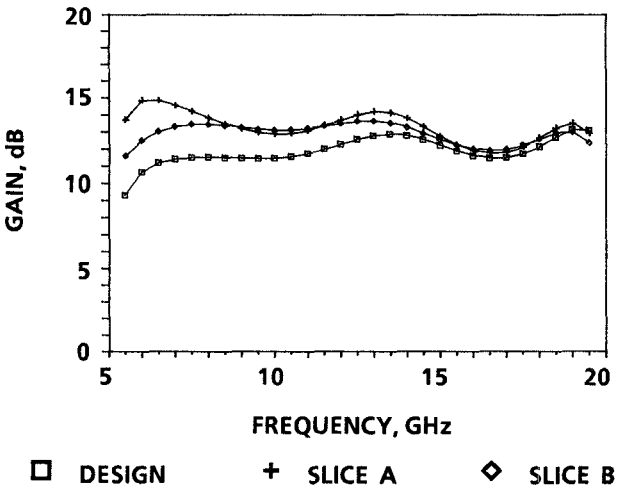

Figure 3. Computer model responses for the original design, slice A, and slice B.

Table 3: Critical Parameter Values
(FET parameters at V_{GS} = -1.0V, V_{DS} = 6.0V)

symbol	units	design assumption	Slice A	Slice B
g_m	mS	50	55	64
C_{gs}	pF	0.33	0.39	0.47
R_{ds}	Ω	250	292	285
r_s	Ω/□	400	552	336
h_s	mils	4.0	3.5	4.0

and the correction of the substrate height brought the worst case gain ripple down from 5.08 dB to 3.55 dB; the average gain ripple for the slice B sample is 3.47 dB.

The changes in g_m, C_{gs}, and r_s suggest a higher implant activation for slice B, and indeed the process monitor C-V measurements did indicate a roughly 20 % increase in the doping density under the gates of the slice B FETs. It is interesting to note that the

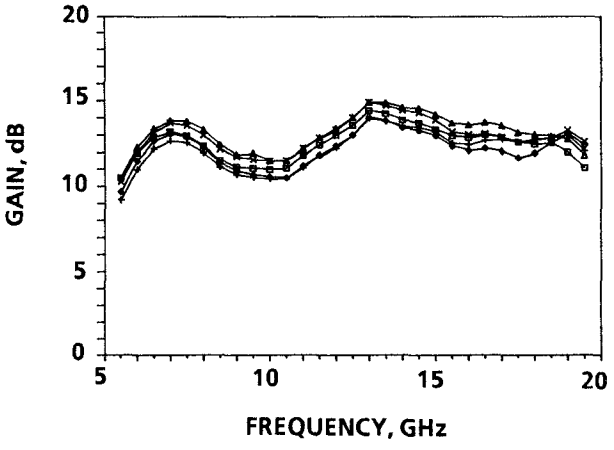

Figure 4. Measured gain responses of selected amplifiers from slice B. All devices measured at V_{GS} = -1.0 V, V_{DS} = +6.0 V.

overall level and slope of the gain responses are similar for the two slices, despite the changes in FET characteristics. Referring to the sensitivity matrix, note that at the high end of the band, the effect of the increase in g_m is partially offset by the increase in C_{gs}; similarly, at the low end of the band, the increase in transconductance tends to be cancelled out by the downward change in r_s. Although we have considered adding a trim etch step to adjust the GaAs resistor values, it appears that allowing the resistors to vary helps reduce the sensitivity of the gain slope to variations in activation.

The sensitivity matrix suggests that a further adjustment to h_s might improve the response. A more recent sample with a 4.5 mil substrate height exhibited 3.27 dB average gain ripple. Further adjustments to h_s would probably increase gain ripple, however, due to a degradation of the input VSWR at the high end of the 6-18 GHz band.

CONCLUSIONS

Our present CAD software does not predict the EG8005 amplifier responses with extreme precision. When combined with the sensitivity analysis approach, however, it is very useful in tracking down problems and identifying ways to refine the small-signal response. This approach has resulted in substantial progress towards the goal of a mass produced, standard, 6-18 GHz gain block.

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